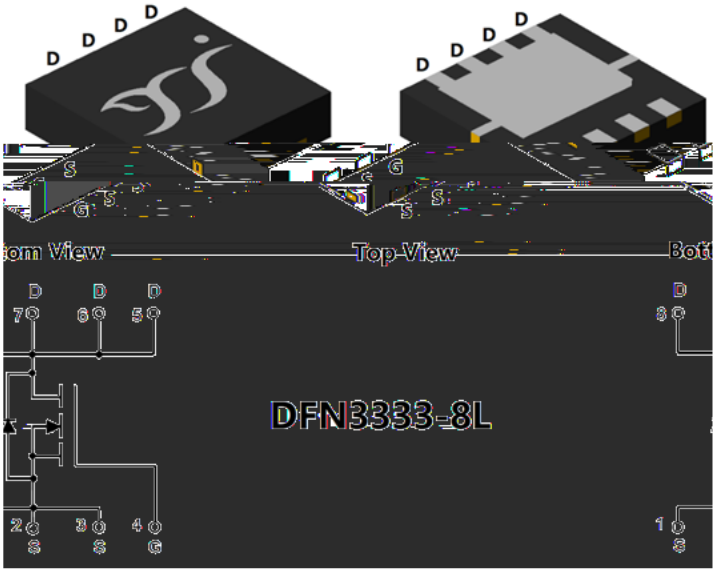
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	40 V
I_D	20 A
$R_{DS(ON)}$(at V_{GS}= 10V)	14.0 mohm
$R_{DS(ON)}$(at V_{GS}= 4.5V)	18.5 mohm

100% EAS Tested
100% V_{DS} Tested
ESD Level (HBM) Class 1B

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
s UL 94 V-0 Flammability Rating
alogen Free

Applications

High current load applications
Load switching
Hard switched and high frequency circuits
Uninterruptible power supply

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	20	V
Drain Current	T_C=25	I_D	20	A
	T_C=100		14	
Pulsed Drain Current [A]		I_{DM}	90	A
Single Pulse Avalanche Energy [B]		E_{AS}	70	mJ
Total Power Dissipation	T_C=25	P_D	21	W
	T_A=25		2.34	
Thermal Resistance Junction-to-Case		R_{JC}	5.9	/ W
		R_{JA}	53.4	
Junction and Storage Temperature Range		T_J , T_{STG}	-55 +150	

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ20N04A	F1	Q20N04	5000	10000	100000	13 reel

YJQ20

Typical Performance Characteristics

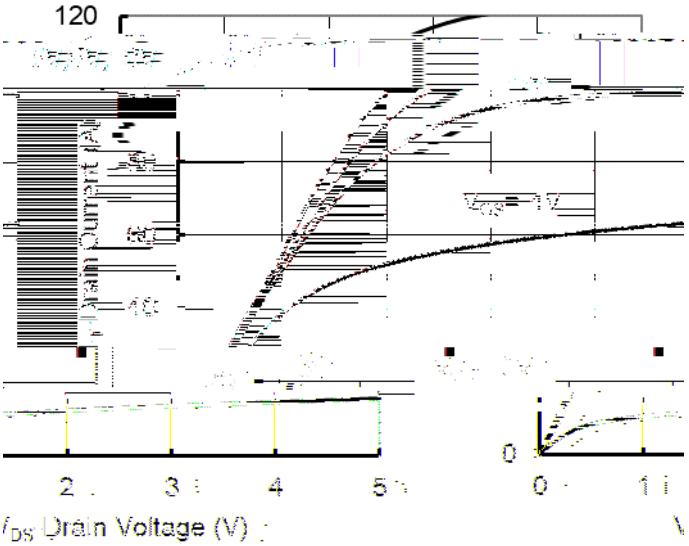


Figure 1. Output Characteristics

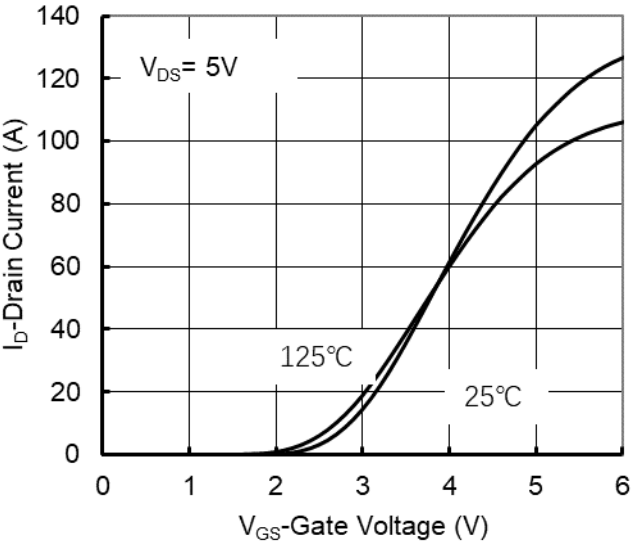


Figure 2. Transfer Characteristics

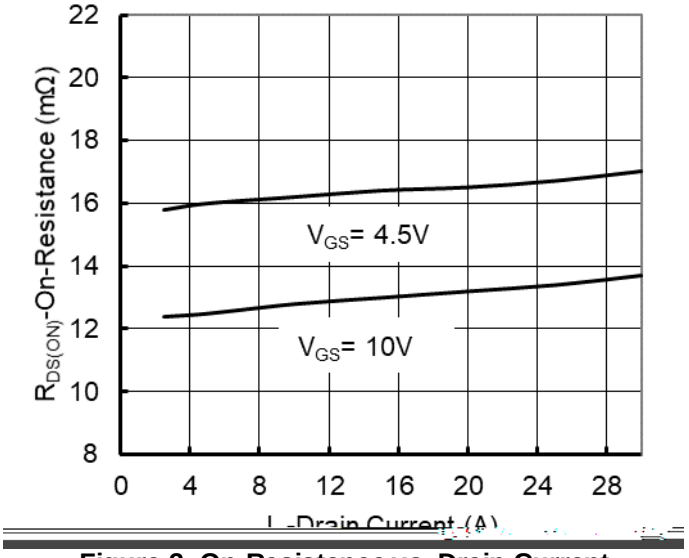


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

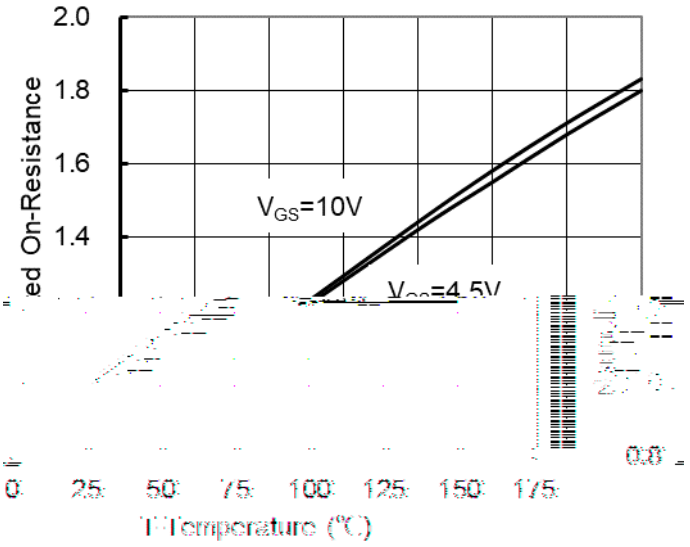


Figure 4. On-Resistance vs. Junction Temperature

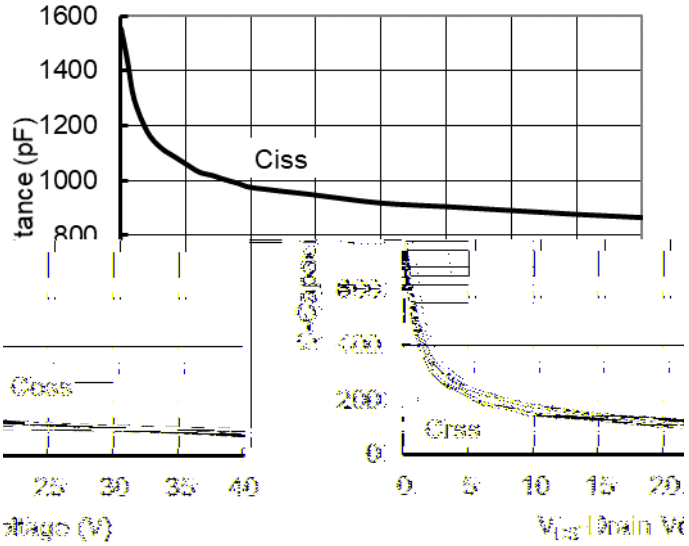


Figure 5. Capacitance Characteristics

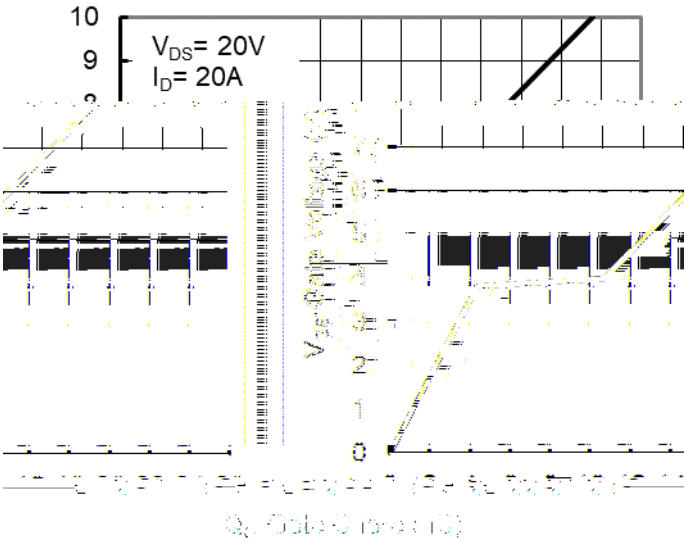
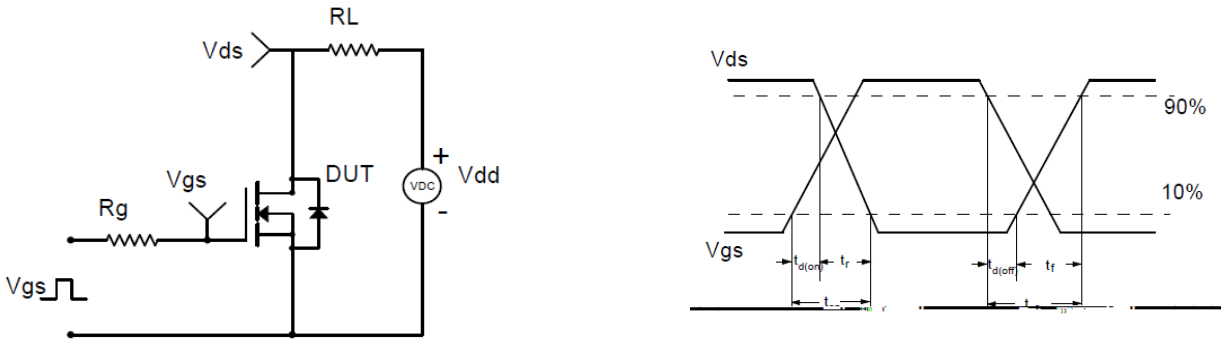
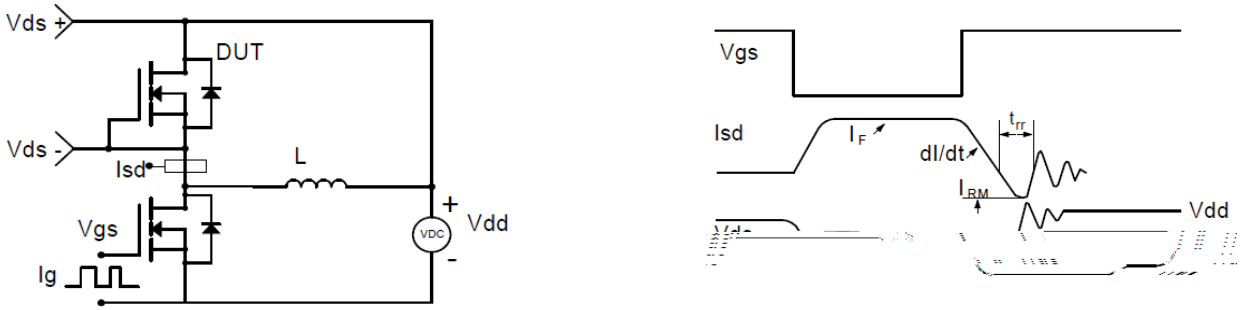


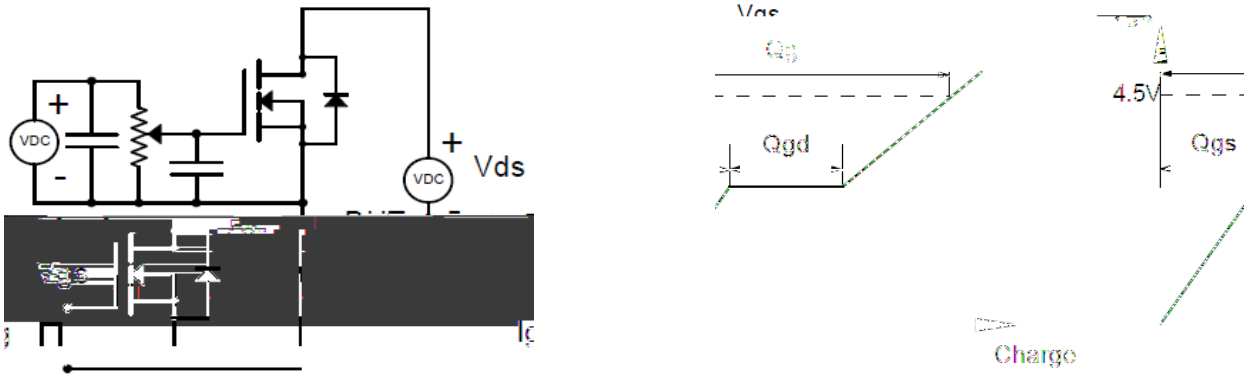
Figure 6. Gate Charge



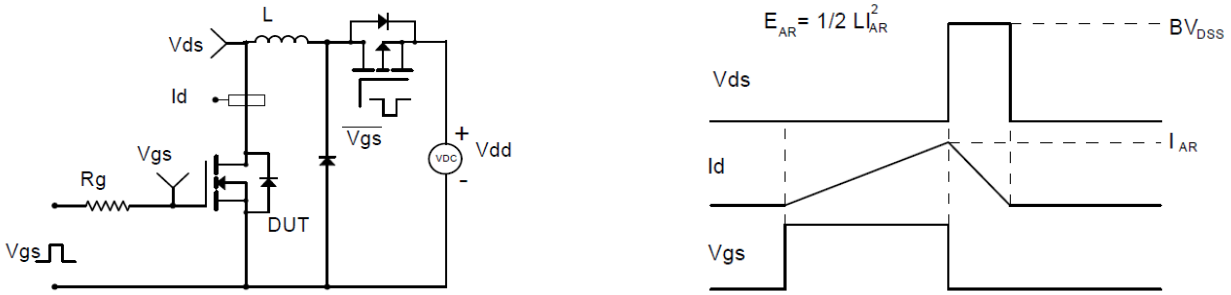
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

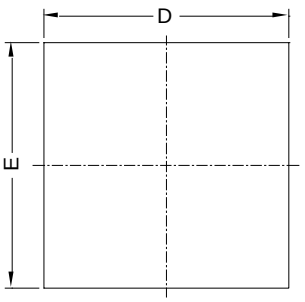


Gate Charge Test Circuit & Waveform

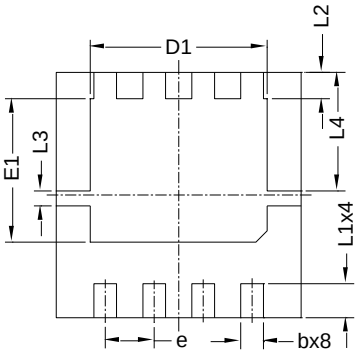


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

DFN3333-8L-A-0.8MM Package information



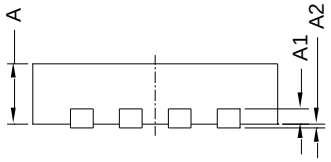
Top View



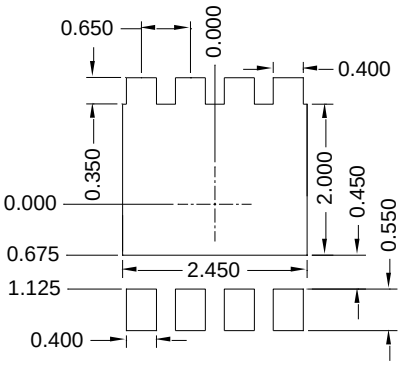
Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2		0.35 BSC	
L3		0.20 BSC	
L4		1.57 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

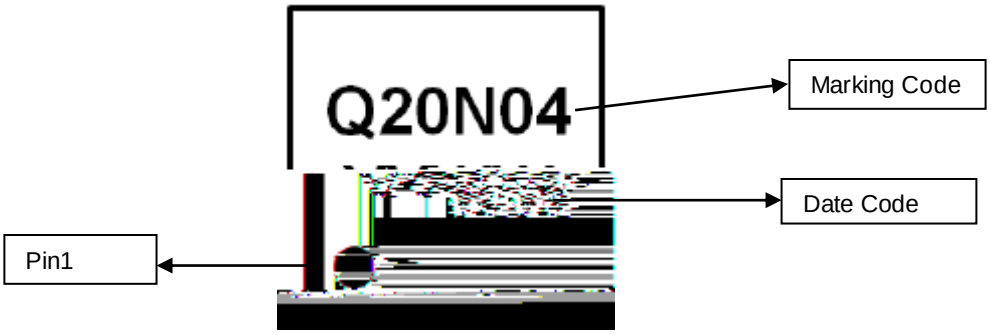


Side View



Suggested Solder Pad Layout
Top View

Marking Information



Note
1. All marking is at middle of the product body
2. All marking is in laser printing
3. Q20N04 is marking code, YYWW is date code,
4. Body color: Black

Ya